

ABSTRACT

A nonvolatile semiconductor memory device having a plurality of electrically rewritable nonvolatile memory cells connected in series together is disclosed. A select gate transistor is connected in series to the serial combination of memory cells. A certain one of the memory cells which is located adjacent to the select gate transistor is for use as a dummy cell. This dummy cell is not used for data storage. During data erasing, the dummy cell is applied with the same bias voltage as that for the other memory cells.